

Advanced Physical Design Program: RTL to GDSII

A 240-hour, competency-based programme that takes you through the complete digital chip implementation flow – from synthesisable RTL to a signed-off, tape-out-ready GDSII database – on industry-standard EDA tools.

240 hrs

CONTACT HOURS

12 weeks

APPROX. DURATION

Sun–Thu

10:00 AM – 2:00 PM

25

SEATS PER BATCH

ABOUT THE PROGRAMME

Industry-aligned, competency-based training

Built on the Skills for Industry Competitiveness and Innovation Program (SICIP) Competency Standard, this programme develops the skills physical design teams hire for. You write and verify RTL, synthesise it, close timing, implement it physically, verify it and sign it off – complete the programme with an RTL-to-GDSII physical design project. Training runs at the ARTIS facility in Dhaka, with a dedicated Linux workstation and EDA environment for every trainee.

RTL Design

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Verification

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Logic Synthesis

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STA

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Physical Design

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Signoff

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GDSII

CURRICULUM

Three stages, ten units

40 hours

Foundations

Semiconductor industry, CMOS & the ASIC flow **16 h**

Linux, EDA tools, Shell/ Tcl & Git **16 h**

Professional communication & design reviews **4 h**

Safe workplace, OHS & ESD practice **4 h**

168 hours

Core Implementation

Synthesisable RTL in Verilog/ SystemVerilog, testbenches & simulation **32 h**

Logic synthesis, SDC constraints, QoR & static timing analysis **36 h**

Physical design: floorplan, power plan, placement, CTS, routing, extraction **52 h**

Physical verification & signoff: DRC, LVS, power, IR drop, signal integrity **24 h**

Advanced techniques: low power, DFT & ATPG, formal, LEC, HLS **24 h**

32 hours

Capstone Project

Plan and execute a complete RTL-to-GDSII implementation, validate it against signoff criteria, document it, and present and defend it before reviewers.

RTL-to-GDSII Physical Design Project

32
HOURS

Plan, execute, validate, document, defend

You plan an RTL-to-GDSII implementation, then execute the complete flow: synthesis, floorplanning, placement, clock tree synthesis, routing and physical optimisation. You validate timing, power, area, DRC, LVS and STA results against signoff criteria, prepare the project documentation and deliverables, and present and defend your design work.

OUTCOMES

What you will be able to do

- Write, simulate and debug synthesisable RTL and self-checking testbenches.
- Synthesise designs, write timing constraints and close timing with STA.
- Floorplan, place, build clock trees and route a block to a clean layout.
- Run DRC, LVS, extraction, power, IR-drop and signal-integrity signoff.
- Apply low-power, DFT, formal and equivalence-checking techniques.
- Automate flows with Shell and Tcl, and manage work in Git.

ASSESSMENT

Competency-based, evidence-led

Each unit is assessed after training against the performance criteria of the SICIP Competency Standard, by certified assessors or occupation-specific industry experts.

Written test

Practical demonstration

Oral questioning

Portfolio (optional)

CAREER PATHWAYS

Where this leads

Physical Design Engineer

STA / Timing Engineer

Synthesis Engineer

Physical Verification Engineer

DFT Engineer

RTL Design Engineer

LEARNING ENVIRONMENT

Built like a design centre

A workstation for every trainee

High-performance Linux machines with individual EDA licences, backed by central licence and file servers.

The full tool chain

Industry-standard tools for simulation, synthesis, STA, place-and-route, physical verification, power and formal analysis.

Real engineering practice

Git-managed projects, scripted flows, design reviews and signoff checklists – the way production teams work.

Learn before the lab

Short video demonstrations ahead of each session, so lab time is spent doing, not watching.

Apply for the next batch

Seats are limited to 25 per batch. Register your interest and we will contact you with the application details.