

SILICON SPRINT

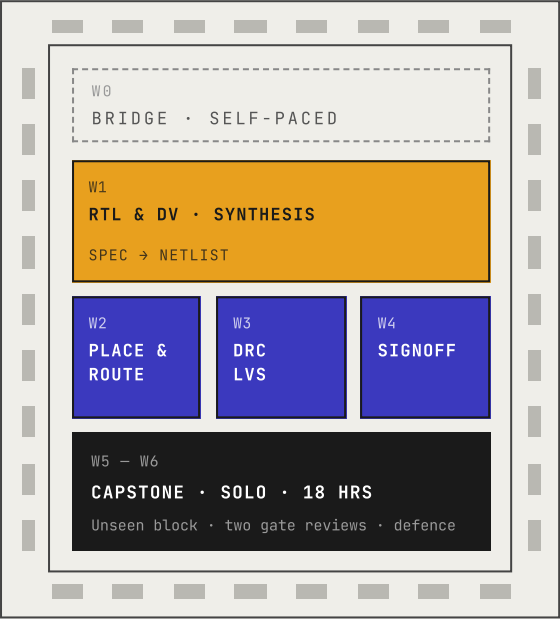
The six-week accelerator that takes any engineering background from a blank file to a signed-off GDSII — and decides their specialisation on evidence rather than an interview.

X1 · ACCELERATOR

DIRECTOR BRIEFING

6 WEEKS · 18 SESSIONS	54 CONTACT HOURS	3x3 HRS/DAY × DAYS/WK	4+1 STAGES + CAPSTONE	7 CADENCE TOOLS	OPEN INTAKE BRIDGE LEVELS THE ROOM
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THE PROGRAMME AS A DIE



- FRONT-END · WEEK 1
- BACK-END · WEEKS 2-4
- CAPSTONE · WEEKS 5-6

One design, carried end to end. A UART-fed FIFO and MAC block is issued on day one; every week's output is the next week's input, so a week week shows immediately rather than at the end.

GRADUATES LEAVE WITH

- A taped-out block.** GDSII they took end to end
- A signoff pack.** Timing, power, DRC/LVS, coverage
- A recorded defence.** Ten minutes before a panel
- A documented repository.** Reviewable by a hiring manager
- A written Lane Report.** Six scores, two gate reviews

AND THE CAPABILITY TO

- Read a spec and write review-ready synthesisable RTL
- Build self-checking testbenches and run regressions
- Constrain and synthesise RTL to a gate-level netlist
- Floorplan, place, clock-tree and route a block
- Run DRC, LVS, extraction, STA and IR-drop signoff

THE LANE REPORT ROUTES INTO

- F2** Digital Design & Verilog Essentials
- S1** Functional Verification — SV & SVA
- S2** RTL Simulation & Logic Synthesis
- S5** Physical Implementation with Innovus
- A2** Static Timing & DFT Signoff
- A5** Physical Verification & Tapeout Signoff

WHAT THE SIX WEEKS COVER

W0	The bridge — before day one Linux, shell and Tcl · digital logic and Verilog refresher · tool login	6 HRS · SELF-PACED
W1	RTL design & verification Spec to synthesisable Verilog · self-checking testbench · waveform debug · SDC constraints · first netlist	XCELIUM · GENUS
W2	Physical design Floorplan and power plan · placement and congestion · clock tree synthesis · routing · post-route timing	INNOVUS
W3	Physical verification DRC rule decks and triage · LVS · antenna and density · parasitic extraction and SPEF	PVS · QUANTUS
W4	Timing & power signoff STA, WNS/TNS and critical paths · ECO closure · IR drop and power integrity · GDSII stream-out	TEMPUS · VOLTUS
W5	Capstone — front-end closure Unseen spec: RTL, verification and synthesis, alone. Ends at gate review 1	SOLO · 9 HRS
W6	Capstone — back-end & defence Route, verify, sign off, stream out · ten-minute panel review · gate review 2 issues the Lane Report	SOLO · 9 HRS

01 — INTAKE ONE DOOR, NOT SIX

Every enquiry enters through a single programme instead of being counselled course by course. Placement becomes a decision made with data.

02 — CONVERSION GRADUATES ARRIVE PREQUALIFIED

They finish knowing the tools, the flow and their own aptitude, so the specialisation course they enrol in next starts at speed.

03 — REPUTATION PORTFOLIOS, NOT CERTIFICATES

Every graduate carries a defended, documented design into the market — the strongest recruitment argument the facility can make.